

ANNOUNCEMENT LETTER

EPIC, a European cooperative research project, started on 1st September 2017 with a set duration of 36 months. It receives funding from The European Union's Horizon 2020 research and innovation program.

EPIC: Enabling Practical Wireless Tb/s Communications with Next Generation Channel Coding

EPIC aims to **develop a new generation of Forward-Error-Correction (FEC) codes** in order to enable practical wireless Terabyte per second (Tb/s) technology. This corresponds to a 10x–100x throughput improvement over the current state-of-the-art. The EPIC concept and methodology is shaped by the key finding that **routine progress in silicon technology in the next decade will not be sufficient** to allow FEC implementations to break the Tb/s barrier. Tb/s FEC will require not only help from silicon technology but also major innovations in FEC algorithm design and implementation domains.

Therefore, a key objective of EPIC is to **develop and utilize a disruptive FEC design** allowing to **advance state-of-the-art FEC schemes** and to obtain the principal channel codes for **beyond-5G (B5G) use-cases**. EPIC will validate and demonstrate the developed FEC technology in **virtual silicon tape-out** and provide a **first-in-class wireless Tb/s FEC chipset** architecture block. Virtual silicon methodologies proved a less time-consuming process during the development of new designs.

Furthermore, EPIC will make major contributions to the scientific community in the fields of **Turbo, LDPC, and Polar code design and implementation**. This collaborative initiative will engage in cross-project activities to maximize the impact of the work, ensure adoption in related work, and **reaffirm Europe's central role in information theory and Digital Signal Processing DSP research**. Industrial partners in EPIC will ensure early identification of commercialization potential and uptake in standardization bodies.

The goals of the EPIC project:

The EPIC consortium, which includes the lead inventors and institutes in the FEC domain, dynamic SMEs, and impactful industry partners, is dedicated to successfully reach the following objectives:

- EPIC will design and implement **next generation Forward-Error-Correction** for wireless Tb/s technology and Beyond-5G systems.
- EPIC will advance state-of-the-art codes and **develop the principal channel coding** technology for wireless Tb/s technology.
- EPIC will **devise a disruptive FEC design framework** to unify algorithmic and implementation domains.
- EPIC will **validate and demonstrate the developed FEC technology** in virtual silicon tape-out and provide first-in-class wireless Tb/s FEC chipset architecture block.
- EPIC puts the **scientific excellence and contributions to wireless industry** in the domain of B5G standardization and technology development at the **centre of the project execution**.

The EPIC consortium consists of **8 partners** from **7 different countries** (Austria, Belgium, France, Germany, Sweden, Turkey and United Kingdom). Due to **excellent cooperation** in the proposal creation phase the basis for a very **promising collaboration has already been set**.

The EPIC partners are:

- TECHNIKON Forschungs- und Planungsgesellschaft mbH, Austria
- InterDigitalEurope Ltd., UK
- Interuniversitair Micro-Electronica Centrum VZW, Belgium
- Polaran Yazilim Bilisim Dan. Ith.Ihr.Tic.Ltd.Sti, Turkey
- Technische Universitaet Kaiserslautern, Germany
- Ericsson AB, Sweden
- Institut Mines-Telecom, France
- Creonic GmbH, Germany

For more information visit www.epic-h2020.eu [coming soon]

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